IT 209 Autumn 2019

Direct Mapped Cache Memory Practice Problem

**Question:**

Consider following two loops written in C, which calculates the sum of the entries in a 128 by 64 matrix of 32 bit integer

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| ***Loop A*** | ***Loop B*** |
| **sum = 0;**  **for (i = 0; i < 128; i++)**  **for (j = 0; j < 64; j++)**  **sum += A[i][j];** | **sum = 0;**  **for (j = 0; j < 64; j++)**  **for (i = 0; i < 128; i++)**  **sum += A[i][j];** |

The matrix is stored contiguously in memory in row-major order. Row major order means that elements in the same row of the matrix are adjacent in memory A[i][j] resides in memory location [4\*(64\*i + j)]

Assume that the caches are initially empty. Also, assume that only accesses to **matrix** cause memory references and all other necessary variables are stored in registers. Instructions are in a separate instruction cache.

Consider a 4KB direct-mapped data cache with 8-word (32-byte) cache lines.

1. Calculate the number of cache misses that will occur when running Loop A.
2. Calculate the number of cache misses that will occur when running Loop B.